PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
THOMAS J. SONDERMAN
PIRAINDER LALL

Serial No.: 10/614,354

Filed: July 7, 2003

For: METHODS OF CONTROLLING PROPERTIES AND CHARACTERISTICS OF A GATE INSULATION LAYER BASED UPON ELECTRICAL TEST DATA, AND SYSTEM FOR PERFORMING SAME

Group Art Unit: 2823

Examiner: Khiem D. Nguyen

Atty. Dkt. No.: 2000.100800/TT5273

Customer No.: 23720

APPEAL BRIEF

CERTIFICATE OF MAILING
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MS APPEAL BRIEF - PATENTS
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated June 21, 2005. The Notice of Appeal for this application was filed on August 9, 2005.

The Director is authorized to deduct the fee for filing this Appeal Brief ($500) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT5273.[1]

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[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.100800.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

1, 3, 6-9, 11-15, 21 and 22 are pending in the application. Claims 1, 3, 6-9, 11-15, 21 and 22 were rejected in the Final Office Action issued on June 21, 2005. Claims 1, 3, 6-9, 11-15, 21 and 22 are the subject of the present appeal. Claims 1, 3, 6-9, 11-15, 21 and 22 are attached as Appendix A.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the present invention is directed to semiconductor fabrication technology, and, more particularly, to various methods of controlling properties and characteristics of a gate insulation layer based upon electrical test data, and a system for performing same. There are four independent claims at issue in the current appeal: claims 1, 9, 21 and 22.

Independent claim 1 is generally directed to a method that involves performing at least one electrical test on at least one flash memory device 10 to determine a duration of a programming cycle performed on the flash memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation

layer 16 on a subsequently formed flash memory device 10 based upon the determined duration of the programming cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed flash memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 9 is generally directed to a method that involves performing at least one electrical test on at least one flash memory device 10 to determine a duration of an erase cycle performed on the flash memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed flash memory device 10 based upon the determined duration of the erase cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed flash memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 21 is generally directed to a method that involves performing at least one electrical test on at least one memory device 10 to determine a duration of a programming cycle performed on the memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed memory device 10 based upon the determined duration of the programming cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed memory device 10.

This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

Independent claim 22 is generally directed to a method that involves performing at least one electrical test on at least one memory device 10 to determine a duration of an erase cycle performed on the memory device 10, determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer 16 on a subsequently formed memory device 10 based upon the determined duration of the erase cycle, and performing the at least one process operation comprised of the determined at least one parameter to form the at least one gate insulation layer 16 on the subsequently formed memory device 10. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 9, l. 1 – p. 11, l. 5; p. 11, l. 12 – p. 15, l. 6; Figure 3.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3 6-9, 11-15, 21 and 22 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Cappelletti (U.S. Patent No. 5,793,675) in view of Wong (U.S. Patent No. 6,882,567).

VII. ARGUMENT

A. Legal Standards

As the Board well knows, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation

of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

B. The Examiner Erred in Rejecting Claims 1, 3, 6-9, 11-15, 21 and 22

The claims at issue in this appeal are directed to methods of forming memory devices whereby the performance of the resulting devices may be enhanced. For example, independent claim 1 recites that the semiconductor device is a flash memory device and that an electrical test is performed to determine a duration of a programming cycle for the flash memory device. Claim 1 further recites that the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed flash memory device is based upon the determined duration of the programming cycle. Independent claim 9 is similar to claim 1 except that the electrical test is performed to determine the duration of an erase cycle for the flash memory device. As noted in the specification, since the characteristics of the gate insulation layer are controlled based upon electrical test data, the completed devices have a better chance of meeting performance criteria that is important to the end users of the final product, *e.g.*, faster erase cycle times. Specification, p. 15, ll. 4-6.

Independent claims 21 and 22 are similar to independent claims 1 and 9, except that independent claims 21 and 22 refer to a generic "memory device," as opposed to the specifically recited "flash memory device" in independent claims 1 and 9.

In rejecting the present claims, the Examiner's primary reference was Cappelletti. Cappelletti is understood to be directed to a test structure that is used in evaluating the quality of gate oxide layers employed in various memory devices. Abstract. In the test structure disclosed therein, all of the cells are connected electrically parallel to one another. Col. 2, l. 64 – Col. 3, l. 12. The structure disclosed therein is electrically stressed in such a manner so as to extract electrons from the floating gate of defective gate oxide cells while the other non-defective cells remain unchanged. Col. 3, ll. 30-46. Cappelletti even discloses stressing the test structure disclosed therein in ramped stages. Col. 4, l. 66 – Col. 5, l. 26. After all the testing is done, if

the difference between resulting VRL and VRH values exceeds a preselected threshold, the structure is considered defective. Col. 5, ll. 32-35.

The Examiner concedes that Cappelletti does not disclose determining the duration of a programming cycle or an erase cycle for a flash memory device, as recited in claims 1 and 9. Final Office Action, p. 3. The Examiner alleges that Cappelletti, at column 3, lines 48-59, discloses the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device based upon electrical test data. Final Office Action, p. 2. It is respectfully submitted that the Examiner's analysis of Cappelletti in this respect is simply wrong. Simply put, the disclosure of Cappelletti cited by the Examiner (Col. 3, ll. 48-59) to support the rejection has nothing to do with the claimed act recited in claims 1 and 9. The passage cited by the Examiner merely describes changes in characteristics of the test structure 10 when it is stressed in accordance with the technique discussed in Cappelletti. At no point does the cited disclosure of Cappelletti even remotely mention or describe the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device based upon electrical test data as alleged by the Examiner.

Although Cappelletti does disclose performing various electrical tests on a test structure to determine the quality of a gate oxide layer, at no point does Cappelletti disclose nor suggest performing at least one electrical test to determine the duration of a programming cycle of a flash memory device or to determine the duration of an erase cycle for a flash memory device. It is not even clear that a programming cycle or an erase cycle could even be performed on the test structure disclosed in Cappelletti. While Cappelletti does disclose that the structure 10 may be subjected to a UV erase procedure, that is not an erase cycle as that phrase is employed and used

in the specification. A plain reading of the specification reflects that the erase cycle disclosed therein is an electrically controlled erasure of the flash memory device. While the cells of the test structure 10 disclosed in Cappelletti are electrically connected parallel to one another, it is not clear that the structure described therein is capable of performing a test to determine the duration of a programming cycle, or the duration of an erase cycle. Simply put, there does not appear to be any associated circuitry with the test structure that would enable the memory cells described therein to be programmed or electrically erased.

As conceded by the Examiner, at no point does Cappelletti even remotely suggest performing an electrical test to determine the duration of a programming cycle for a flash memory device or to determine the erase cycle for a flash memory device. Moreover, Cappelletti does not disclose or suggest determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently manufactured device based upon this determined programming cycle or erase cycle as set forth in the various claims set forth in the application.

In an attempt to cure the fundamental deficiencies in Cappelletti, the Examiner cited Wong as alleged evidence that there is a relationship between threshold voltage and the duration of a programming cycle. Final Office Action, p. 6. As understood by the undersigned, the cited passage of Wong is far from clear in this respect. However, even if true, the Wong reference does not cure the fundamental deficiencies in Cappelletti, as outlined above. More specifically, even if the references were combined in the manner suggested by the Examiner, that combination would still not teach every limitation of the claimed invention. Thus, the Examiner's obviousness rejection is legally improper.

A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. It is respectfully submitted that, in asserting that the pending claims would have been obvious in view of Cappelletti and Wong, the Examiner engaged in an improper use of hindsight using Applicants' disclosure as a roadmap.

Although Cappelletti does disclose performing electrical tests on the test structure disclosed therein to determine various characteristics of a gate oxide layer, at no point does Cappelletti disclose or suggest determining ultimate performance characteristics of a memory device, *e.g.*, the duration of a programming cycle or the duration of an erase cycle, as set forth in the pending claims. Simply put, the pending claims involve determining an ultimate performance characteristic of a memory device, and, based upon that ultimate performance characteristic, determining a parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device. By using the duration of the programming cycle and the duration of the erase cycle to determine processing parameters for the formation of gate insulation layers on subsequently formed memory devices, the production of memory devices that meet ultimate performance specifications can be improved.

The arguments set forth above apply equally as well to independent claims 21 and 22.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1, 3, 6-9, 11-15, 21 and 22 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing claims 1, 3, 6-9, 11-15, 21 and 22 over the prior art of record. Applicants respectfully request the Board reverse the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4055 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON
CUSTOMER NO. 23720

Date: October 6, 2005

J. Mike Amerson
Reg. No. 35,426
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-4055
(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANT

APPENDIX A

1. A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of a programming cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

3. The method of claim 1, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and an erase cycle time.

6. The method of claim 1, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

7. The method of claim 1, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

8. The method of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

9. A method, comprising:

performing at least one electrical test on at least one flash memory device to determine a duration of an erase cycle performed on said flash memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed flash memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed flash memory device.

11. The method of claim 9, wherein performing said at least one electrical test on said at least one flash memory device further comprises performing said at least one electrical test on said at least one flash memory device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, and a programming cycle time.

12. The method of claim 9, wherein said memory device is comprised of a gate insulation layer, a floating gate layer positioned above said gate insulation layer, an intermediate

insulation layer positioned above said floating gate layer, and a control gate layer positioned above said intermediate insulation layer.

13. The method of claim 9, wherein said at least one process operation is comprised of at least one of a deposition process and a thermal growth process.

14. The method of claim 9, wherein said at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate, a process gas composition, a liquid flow rate, a liquid composition, and a power level setting.

15. The method of claim 9, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride.

21. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said programming cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.

22. A method, comprising:

performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on said memory device;

determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon said determined duration of said erase cycle; and

performing said at least one process operation comprised of said determined at least one parameter to form said at least one gate insulation layer on said subsequently formed memory device.